CONSONANCE

Low Power Microprocessor Supervisory IC With Watchdog Timer and Manual Reset

CN825 Series

General Description：

CN825 series is a family of microprocessor (uP) supervisory circuit that monitors microprocessor's supply voltage and battery voltage. The CN825 series integrates uP reset circuit with 200ms delay, Watchdog, manual reset circuit. These devices reduce system complexity, hence improve system reliability.

CN825 series generates a reset signal when VCC is lower than reset threshold. The reset threshold is internally fixed with 1% accuracy. The watchdog timer's timeout period is internally set at typical value of 1.6s. CN825 series provide both active low and active high reset signals.

CN825 series is ideal for applications in automotive systems, computers, controllers and intelligent instruments.

All devices are available in 6 pin SOT-23 package.

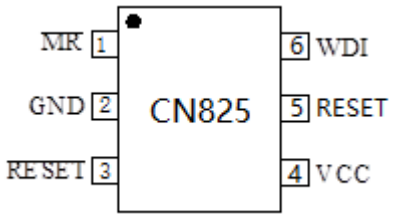
Applications：

- DSP, Computers, Controllers
- Industrial Equipment
- Intelligent instruments
- Battery-powered Equipment

Features：

- Reset Threshold is Internally Fixed
- Guaranteed Reset Valid at VCC=1.1V
- Reset threshold can be from 1.8V to 5.0V with 0.1V step.
- High Accuracy of Reset Threshold: ±1%
- Low operating current: 2.7uA
- Reset pulse width: 200ms Typical
- Watchdog timer: 1.6s timeout
- Both Active-high and Active-low Reset Outputs
- Power-Supply Transient Immunity
- Available in SOT-23-6
- Operating Temperature Range
- -40°C to +85°C
- Lead-free, Rohs-compliant and Halogen-free

Pin Assignment:



Typical Application Circuit:

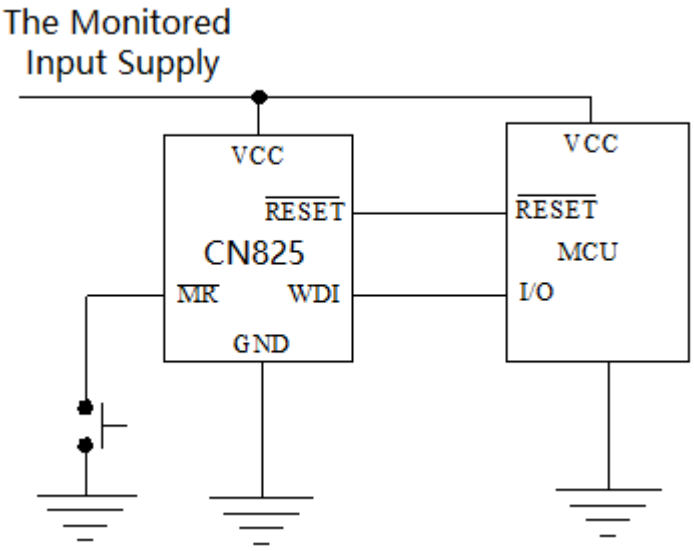


Figure 1 Typical Application Circuit

Device Function Reference Table

Part No.	Reset Threshold	Reset Active	Marking	Operating Temperature
CN825S	2.93V	Low and High	825S	－40℃--85℃
CN825R	2.63V	Low and High	825R	－40℃--85℃
CN825Z	2.32V	Low and High	825Z	－40℃--85℃

Note: Please contact our sales office for other reset threshold from 1.8V to 5.0V

Ordering Information：

Part No.	Package	Shipping	Operating Temperature Range
CN825X	SOT23-6	Tape and Reel, 3000/Reel	－40℃ to 85℃

Note: “X” stands for L, M, T, S, R, Z, Y

Block Diagram:

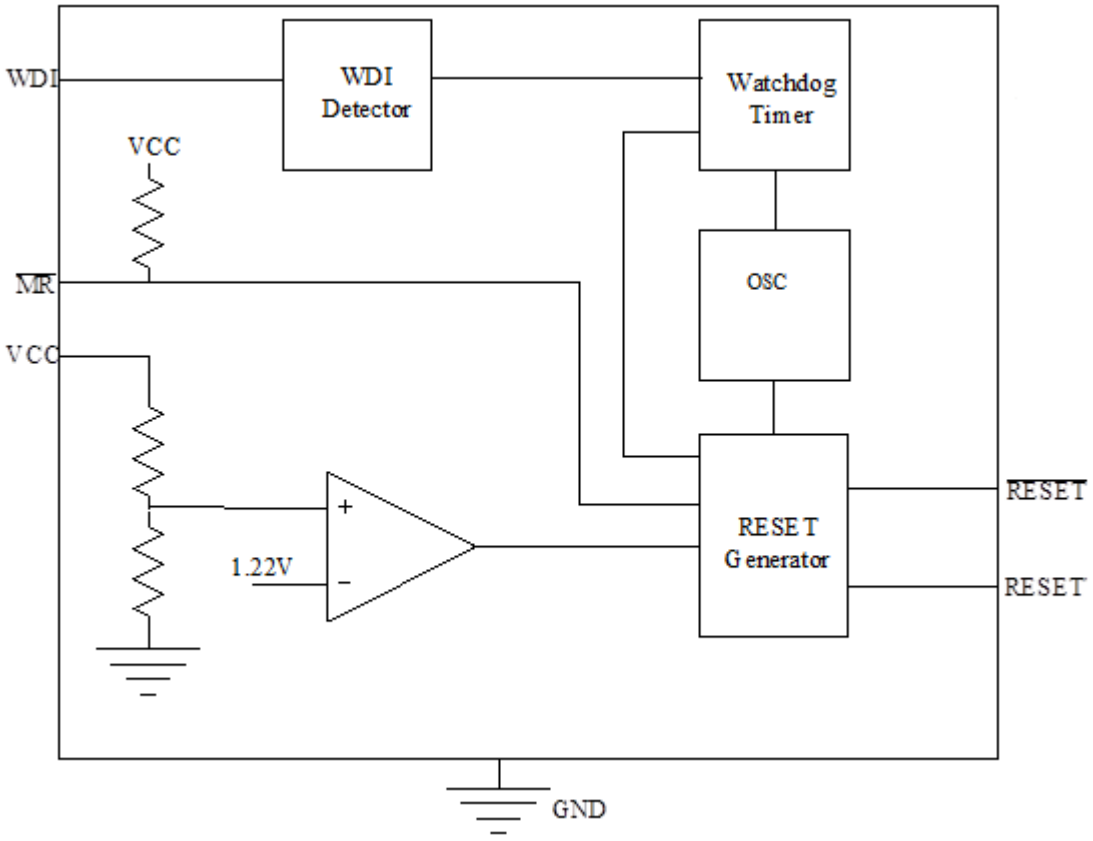


Figure 2 CN825 block Diagram

Pin Description：

Pin No.	Symbol	Description
1	$\overline{MR}$	**Manual Reset Input.** When voltage at $\overline{MR}$ is pulled low, a reset pulse will be triggered. The active low input has a pull-up resistor of 50K ohm, so it can be left open if not used. This input can be driven with CMOS logic levels or with open-drain/ collector outputs.
2	GND	**Negative Terminal of Power Supply.** Namely the Ground of the chip.
3	$\overline{RESET}$	**Active Low Reset Output.** $\overline{RESET}$ stays in low if VCC is lower than reset threshold or $\overline{MR}$ is low level or watchdog timer times out; it remains in low for 200ms (Typical) after VCC becomes higher than reset threshold or $\overline{MR}$ goes from low to high or after watchdog timer time out.
4	VCC	**Positive Terminal of Power Supply.** The CN825 is powered through this pin, and the voltage of this pin is monitored.
5	RESET	**Active High Reset Output.** RESET is the inverse of $\overline{RESET}$. RESET stays in high if VCC is lower than reset threshold or $\overline{MR}$ is low level or watchdog timer times out; it remains in high for 200ms (Typical) after VCC becomes higher than reset threshold or $\overline{MR}$ goes from low to high or after watchdog timer time out.
6	WDI	**Watchdog Input.** If WDI remains high or low for 1.6s (Typical), the on chip watchdog timer runs out and $\overline{RESET}$ pin goes low, RESET pin goes high. If active reset pulse is not expected, the WDI input must see a level transition from low to high or from high to low.

Absolute Maximum Ratings：

Terminal Voltage(With respect to GND)：
VCC……-0.3V to 6.5V
Other Inputs ……..……..-0.3V to VCC
Terminal Current
VCC…….20mA
All I/O Pins……...…..20mA

Thermal Resistance……..……220℃/W
Storage Temperature…….....－65℃ to 150℃
Maximum Junction Temperature…….....150℃
Operating Temperature……..－40℃ to 85℃
Lead Temperature(Soldering, 10s)……..260℃

Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

Electrical Characteristics：

(VCC=3V, T_A=－40℃ to 85℃, Typical values are measured at T_A=25℃,unless otherwise noted)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage Range	VCC		1.1		6.5	V
Supply Current	I_{VCC}	VCC is below threshold	2	2.7	3.7	uA
		VCC is over threshold	10	16	22	
Reset Threshold	V_{RES}	CN825L, VCC falls	4.58	4.63	4.68	V
		CN825M, VCC falls	4.33	4.38	4.43	
		CN825T, VCC falls	3.04	3.08	3.12	
		CN825S, VCC falls	2.9	2.93	2.96	
		CN825R	2.60	2.63	2.66	
		CN825Z, VCC falls	2.297	2.32	2.343	
		CN825Y, VCC falls	2.168	2.19	2.212	
Reset Threshold Hysteresis	H_{VRES}			$0.02V_{RES}$		V
Reset Pulse Width	t_{RES}		140	200	280	ms
$\overline{RESET}$ or RESET Output Voltage	V_{OH1}	I_{SOURCE}=1mA	VCC－1			V
		I_{SOURCE}=8uA,VCC=1.1V	1.0			
	V_{OL1}	I_{SINK}=3.2mA			0.3	V
		I_{SINK}=150uA,VCC=1.1V			0.3	
Watchdog timeout period	t_{WD}		0.95	1.6	2.25	s
WDI Pin						
WDI Input Current	I_{WDI}		-50		+50	nA
WDI Pulse Width	t_{WP}		50			ns
WDI Input Threshold		Low			0.25*VCC	V
		High	0.75*VCC			
$\overline{MR}$ **Pin**						
$\overline{MR}$ Pull-up Resistance			38	50	62	KΩ
$\overline{MR}$ Pulse Width	T_{MR}		1			us
$\overline{MR}$ Input Threshold		Low			0.25*VCC	V
		High	0.75*VCC			
$\overline{MR}$ to RESET Delay	t_{MD}				500	ns

Detailed Description：

CN825 series are microprocessor supervisory circuits that monitor the power supply to digital circuits such as microprocessor, controller, DSP and memory . The CN825 asserts reset during power up, power down or brownout condition to prevent code execution errors.
CN825 series reset thresholds are internally fixed with 1% accuracy.

$\overline{\text{RESET}}$ and RESET output

On power up, once VCC reaches 1.1V, CN825 series output reset signals, active-high RESET and active-low $\overline{\text{RESET}}$. As VCC increases, the reset signal stays valid; When VCC rises above reset threshold, an internal timer releases RESET ($\overline{\text{RESET}}$) after 200ms (Typical). RESET ($\overline{\text{RESET}}$) becomes valid once VCC dips below reset threshold during power down or in brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse will continue for at least another 140ms. On power down, once VCC falls below reset threshold, reset signals stay valid and are guaranteed in the correct logic state until VCC drops below 1.1V for the whole temperature range.

Watchdog Timer

CN825 series have a watchdog timer that can monitor uP's activity. If uP does not toggle the watchdog input (WDI) within 1.6s(Typical), the watchdog timer runs out, the reset outputs are asserted, and stays in valid for at least 140ms. When VCC stays below reset threshold or $\overline{\text{MR}}$ stays logic low, the watchdog timer is cleared.
The minimum pulse width of WDI is 50ns.

Manual Reset

Many μP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the CN825, a logic low on $\overline{\text{MR}}$ pin asserts reset. Reset remains asserted while $\overline{\text{MR}}$ is low, and for t_{RES} (200ms nominal) after it returns high. $\overline{\text{MR}}$ pin has an internal 50kΩ pull-up resistor, so it can be left open if not used. This input can be driven with CMOS logic levels or with open-drain/ collector outputs. Connect a normally open momentary switch from $\overline{\text{MR}}$ pin to GND to create a manual-reset function; external de-bounce circuitry is not required. If $\overline{\text{MR}}$ pin is driven from long cables or the device is used in a noisy environment, connect a 0.1μF capacitor from $\overline{\text{MR}}$ pin to GND to provide additional noise immunity.

The CN825 series's operation can be best understood by the timing diagram in Figure 3 and Figure 4.

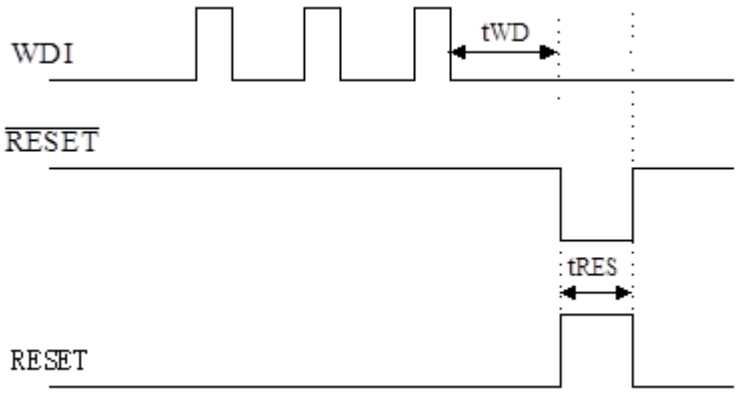


Figure 3　Watchdog Timing

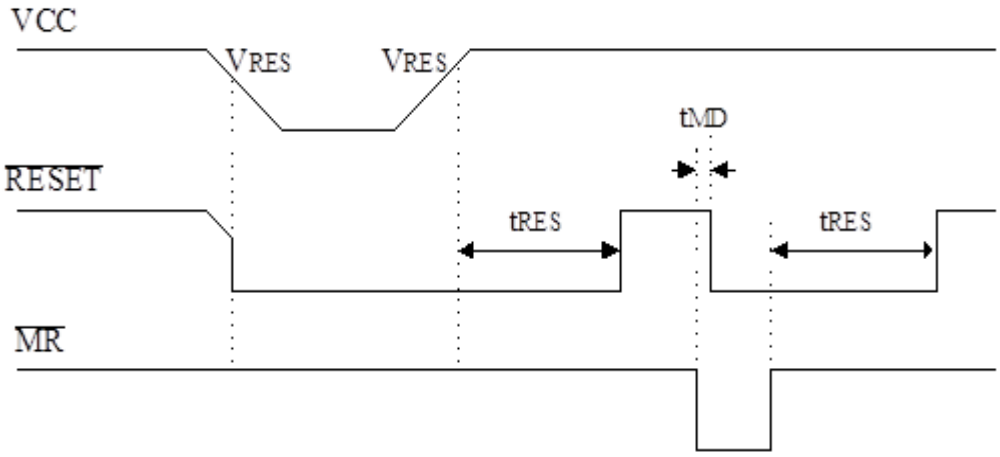


Figure 4 Reset Timing

Application Information

Ensuring Valid Reset Outputs Down to VCC=0V

When VCC falls below 1.1V, the CN825 series $\overline{\text{RESET}}$ and RESET outputs no longer sinks or sources current, it becomes an open circuit, hence the 2 reset outputs are at undetermined voltage. If a pull-down resistor is added from $\overline{\text{RESET}}$ pin to GND and a pull-up resistor is added from RESET pin to VCC as shown in Figure 5, then $\overline{\text{RESET}}$ and RESET outputs will be held at active state. The resistor's value is not critical. it should be around several hundred kilo-ohm., large enough not to load $\overline{\text{RESET}}$, small enough to pull the reset outputs to active level.

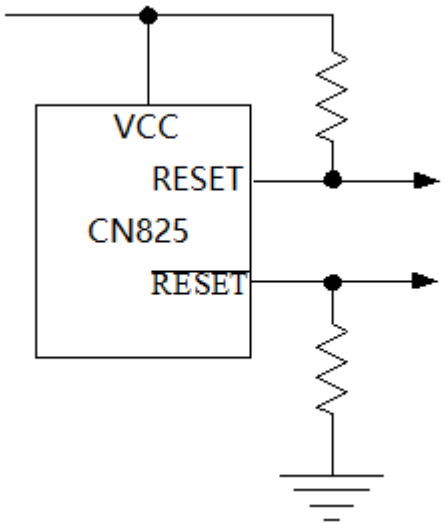


Figure 5 To Ensure Valid Reset Outputs Down to VCC=0V

Negative-Going VCC Transients

The CN825 series are relatively immune to short duration of negative-going VCC transients (glitches), which usually do not require the entire system to reset.

The maximum pulse width that a negative-going VCC transient can typically have without triggering a reset pulse is listed in Table 1 versus the amplitude of the transient. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Here the amplitude of the transient means the voltage the transient's lowest level is below reset threshold.

Table 1

Amplitude of Negative-Going Transient	Maximum Pulse Width
10mV	25us
20mV	13us
50mV	8us
100mV	5us

An optional 0.1μF bypass capacitor mounted close to VCC provides additional transient immunity.

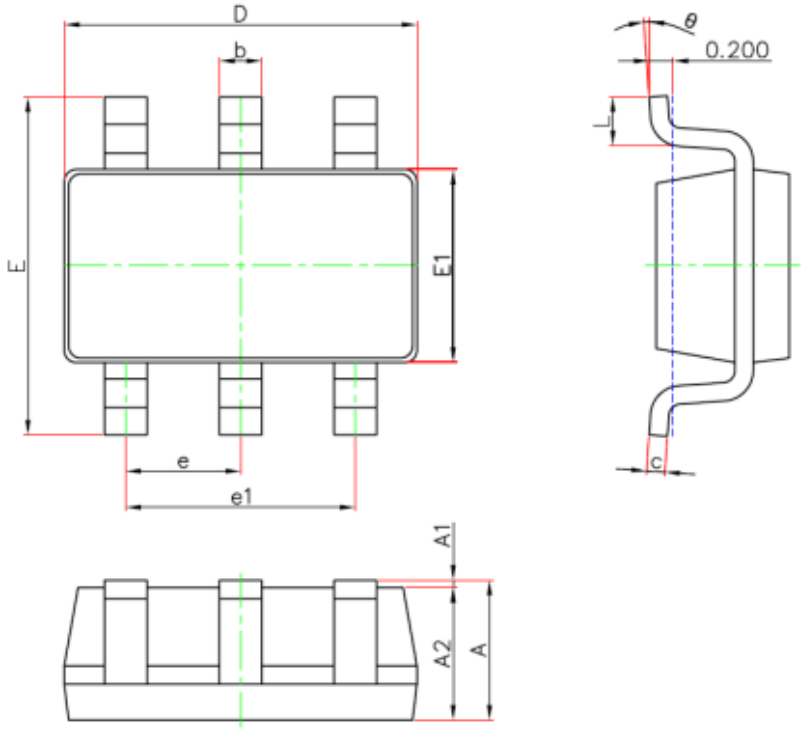
Watchdog Software Considerations

The microprocessor's software should set and reset the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset inside the loop, keeping the watchdog from timing out.

To make sure the watchdog timer does not run out in normal operation, the time interval between 2 consecutive toggles on watchdog input (WDI pin) should be less than the minimum watchdog timeout period which is 0.95s.

Package Information

SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°